

United States Patent and Trademark Office



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FIL	ING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,566	10/678,566 10/03/2003		Jalal Hallak	MAT-0003	3587
33941	7590	10/10/2006		EXAMINER	
MONTE &			WILLOUGHBY, TERRENCE RONIQUE		
	4092 SKIPPACK PIKE P.O. BOX 650				PAPER NUMBER
SKIPPACK, PA 19474				2836	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/678,566	HALLAK ET AL.				
Office Action Summary	Examiner	Art Unit				
	Terrence R. Willoughby	2836				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. sely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
 Responsive to communication(s) filed on 6/30/2 This action is FINAL. 2b) This Since this application is in condition for allowar closed in accordance with the practice under E 	action is non-final. nce except for formal matters, pro					
Disposition of Claims	.,					
4) Claim(s) 1,2 and 4-7 is/are pending in the appliance of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) 1,2,4,5 and 7 is/are rejected. 7) Claim(s) 6 is/are objected to. 8) Claim(s) are subject to restriction and/or are subject to restriction and/or are subject to by the Examine. 10) The specification is objected to by the Examine. 10) The drawing(s) filed on 30 June 2006 is/are: a) Applicant may not request that any objection to the or Replacement drawing sheet(s) including the correction.	vn from consideration. r election requirement. r. accepted or b) objected to drawing(s) be held in abeyance. See ion is required if the drawing(s) is objected to drawing(s) is objected.	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).				
	ammer. Note the attached office	7.000110110111111101102.				
Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/24/06.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

DETAILED ACTION

Applicant's amendment filed on 6/30/2006 has been entered. Accordingly claims 1,2,4 and 7 have been amended and claim 3 has been cancelled. No new claims were added. It also included remarks/arguments.

Claim Objections

- 1. Claim 1 is objected to as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 2. Regarding claim 1, the phrase "at least on series circuit of an auxiliary semiconductor switch (H1A), likewise triggered by the monitoring unit (UWE) **and** a ballast resistor (RA1)" is unclear and misunderstood how the ballast resistor (RA1) is doing the triggering to the auxiliary semiconductor switch (H1A) when the gate of the auxiliary semiconductor switch (H1A) is connected to the input of the monitoring unit (UWE).
- 3. Claim 6 is objected to as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 4. Regarding claim 6, the phrase "the gate of the main semiconductor switch (SW1) being connected to the **source** and triggered by an output of the monitoring unit (UWE) via a zener diode (ZD1) " is misunderstood how the gate of the main semiconductor is connected?

Application/Control Number: 10/678,566 Page 3

Art Unit: 2836

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

- 6. Claims 1,2,4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duffy (US 5,737,160) and in view of Thomas (US 5,805,393) and Gehl (DE 3432680).
- 7. Regarding claim 1, Duffy discloses (Fig. 10) a power supply (12) in which a feed voltage (U_s) is routed through at least one longitudinal branch to at one output (14), the at least one branch having a disconnect fuse formed as a mechanical switch (6), wherein at least one series circuit of an auxiliary mechanical switch (4), and a PTC resistor (2), is connected in parallel to the mechanical switch (6) and in the event of an overcurrent (column 10, II. 25-31) absorbs a substantial portion of the overload current in the branch (column 11, II. 51-column 12, II. 1-10). Duffy discloses a (PTC) resistor formed as a composite carbon conductive material that performs the same function as a ballast resistor (column 2, II. 4-41).

Duffy does not disclose the mechanical switches (4,6) are semiconductor switches.

However, Thomas discloses an overcurrent protection circuit with a PTC trip endurance (Abstract) that uses bypass semiconductor switches, such as FET types (column 2, II. 66-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the mechanical switches of Duffy with the power semiconductor switches (FET's) taught by Thomas because of their simplicity and reduction in cost.

Duffy and Thomas does not disclose the monitoring unit (UWE) being set up to supply a disconnect signal (s1) to the semiconductor switch when there are changes in voltage or current beyond pre-definable tolerances.

However, Gehl (Fig. 1), discloses a protection circuit against overload and short circuit comprising a monitoring unit (T2) that measures the current through the controllable semiconductor switch (T1) and set up to supply a disconnect signal to the semiconductor switch when there are changes in voltage or current (i.e. overload or short circuit) beyond pre-definable tolerances. (Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a monitoring unit taught by Gehl to the electrical switching arrangement and PTC device of Duffy and Thomas to prevent shut down of circuit due to brief and long-term transient overcurrent conditions.

8. Regarding claim 2, Duffy in view of Thomas and in view of Gehl discloses the claimed said power supply as described in claim 1. Gehl (Fig. 1), discloses the monitoring unit is set up to keep the auxiliary semiconductor circuit (T3, RP) at least substantially disconnected during normal operation, but to switch it on in the event of an overload while simultaneously disconnecting the main semiconductor switch (T1) (Abstract).

Application/Control Number: 10/678,566 Page 5

Art Unit: 2836

9. Regarding claim 4, Duffy in view of Thomas and in view of Gehl discloses the claimed said power supply as described in claim 1. Gehl (Fig. 1), discloses wherein the pre-definable short-circuit current of the branch is essentially determined by the ballast resistor (Rp) and the feed voltage (U), so that R1A \approx U_S/I_{K1}.

- 10. Regarding claim 7, Duffy in view Thomas and in view of Gehl discloses the claimed said power supply as described in claim 1. Duffy discloses a (PTC) resistor formed as a composite carbon conductive material that performs the same function as a ballast resistor (column 2, II. 4-41). Gehl (Fig. 1) also discloses a ballast resistor (RP) is formed as a composite carbon resistor.
- 11. Regarding claim 5, Duffy in view Thomas and in view of Gehl discloses the claimed said power supply as described in claim 1. Thomas discloses bypass semiconductor switches, such as FET types are used in overcurrent protection (column 2, II. 66-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the mechanical switches of Duffy with the power semiconductor switches (FET's) taught by Thomas because of their simplicity and reduction in cost.

Allowable Subject Matter

9. Claim 6 objected to as being dependent upon a rejected base claim 5, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2836

The following is a statement of reasons for the indication of allowable subject matter: Combined claim 6 would be allowable over the art of record because the prior art does not teach the semiconductor switches are of the self-locking FET type, the gate of the main semiconductor switch being connected to the source and triggered by an output of the monitoring unit via a zener diode and the gate of the auxiliary semiconductor switch being triggered directly by the same output as set forth in the claimed invention.

Response to Arguments

12. Applicant's arguments with respect to claims 1,2,4,5 and 7 have been considered but are most in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jehlicka et al. (US 6,710,698) discloses a semiconductor fuse for electrical consumers. Seiler (US 4,186,418) discloses an overvoltage protected integrated circuit network, to control current flow through resistive or inductive loads (abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

Application/Control Number: 10/678,566 Page 7

Art Unit: 2836

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571/272-2800 ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

TRW 9/19/06 BRIAN SIRCUS

SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2000